TechWiz

VLSI Based Project Titles

S. No.	Project Title
1.	Design and implementation of solar robot controlling and storage of energy based on FPGA
2.	Design and Implementation of Area-optimized 256-bit Advanced Encryption Standard for real time images on FPGA
3.	Design and VLSI Implementati on of High-Performance Face- Detection Engine for Mobile Applications
4.	Feature Extraction of Digital Aerial Images by FPGA based implementation of edge detection algorithms
5.	Design and VLSI Implementati on of High-Performance Face-Detection Engine for Mobile Applications
6.	Design and Implementation of Adaptive filtering algorithm for Noise Cancellation in speech signal on FPGA
7.	Hardware Efficient Architecture for Generating Sine/Cosine Waves
8.	A Novel Architecture for VLSI Implementation of RSA Cryptosystem
9.	*Design and Implementation of Reed Solomon Decoder for 802.16 Network using FPGA*
10.	A Dynamic Partial Reconfigurable FIR Filter Architecture
11.	Fully Parallel and Fully Serial architecture for realization of high speed FIR Filters with FPGA's.

12.	Design of Plural-Multiplier Based on CORDIC Algorithm for FFT Application
13.	Area-Efficient VLSI Implementation for Parallel Linear-Phase FIR Digital Filters of Odd Length Based on Fast FIR Algorithm
14.	Distributed Arithmetic LMS Adaptive Filter Implementation without Look-Up Table
15.	Design and Functional Verification of I2C Master Core using OVM
16.	Design & Implementation of Floating point ALU on a FPGA Processor
17.	FPGA Design of a Fast 32-bit Floating Point Multiplier Unit
18.	*Design and Simulation of 32-Point FFT Using Radix-2 Algorithm for FPGA Implementation*
19.	A New Approach for High Performance and Efficient Design of CORDIC Processor
20.	IMPLEMENTATION OF GENERALIZED DFT ON FIELD PROGRAMMABLE GATE ARRAY
21	DESIGN AND IMPLEMENTATION OF DEMODULATION TECHNIQUE WITH COMPLEX DPLL USING CORDIC ALGORITHM
22	FPGA Implementation of Encoder for (15, k) Binary BCH Code Using VHDL and Performance Comparison for Multiple Error Correction Control
23	Area-Time Efficient Scaling-Free CORDIC Using Generalized Micro-Rotation Selection
24	Performance Efficient FPGA Implementation of Parallel 2-D MRI Image Filtering Algorithms using Xilinx System Generator
25.	VLSI Implementation of Autocorrelator and CORDIC algorithm for OFDM based WLAN
26.	High Speed ASIC Design of Complex Multiplier Using Vedic Mathematics
27.	A Novel LMS Algorithm Applied to Adaptive Noise Cancellation
28.	ADAPTIVE NOISE REDUCTION SCHEME FOR SALT AND PEPPER
29.	Field Programmable Gate Array Implementation of Reed-Solomon Code, RS(255,239)
30.	AN EFFICIENT VITERBI DECODER

31.	Fuzzy PID Controllers Using FPGA Technique for Real Time DC Motor Speed Control
32.	FPGA Synthesis of Fuzzy (PD and PID) Controller for Insulin Pumps in Diabetes Using Cadence
33.	Designing & FPGA Implementation of IIR Filter Used for detecting clinical information from ECG
34.	FPGA-based High-speed True Random Number Generator for Cryptographic Applications
35.	FPGA BASED RANDOM NUMBER GENERATION FOR CRYPTOGRAPHIC APPLICATIONS
36.	Field Programmable Gate Array Implementation of Parts-based Object Detection for Real Time Video Applications
37.	A DISTRIBUTED CANNY EDGE DETECTOR AND ITS IMPLEMENTATION ON FPGA
38.	*Design and Implementation of Area-optimized AES Based on FPGA*
39.	FPGA based FFT Algorithm Implementation in WiMAX Communications System
40.	FPGA-BASED CONTROL OF THERMOELECTRIC COOLERS FOR LASER DIODE TEMPERATURE REGULATION
41.	Forward Converter with FPGA-Based Self-Tuning PID Controller
42.	Design and Implementation of Edge Detection Algorithm in dsPIC Embedded Processor
43.	FPGA BASED DIRECT DIGITAL SYNTHESIS FUNCTION GENERATOR
44.	FPGA Based Area Efficient Edge Detection Filter for Image Processing Applications
45.	Design Space Exploration for Sparse Matrix-Matrix Multiplication on FPGAs
46.	FPGA Implementation of Discrete Wavelet Transform (DWT) for JPEG 2000

47.	DESIGN OF LOW POWER AND HIGH SPEED CONFIGURABLE BOOTH MULTIPLIER
48.	A New VLSI Architecture of Parallel Multiplier–Accumulator Based on Radix-2 Modified Booth Algorithm
49.	A Memory-Efficient and Highly Parallel Architecture for Variable Block Size Integer Motion Estimation in H.264/AVC
50.	Improvement of the Orthogonal Code Convolution Capabilities Using FPGA Implementation
51.	*Image Encryption Based On AES Key Expansion*
52.	High-Throughput, Lossless Data Compression on FPGAs
53.	FPGA Implementations of the Hummingbird Cryptographic Algorithm
54.	Face Detection and Recognition Method Based on Skin Color and Depth Information
55.	BPSK System on Spartan 3E FPGA

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